REMARKS

Claims 1, 3, 4, 5 and 16-19 are pending in the application.

Claims 6-15 were previously cancelled without prejudice or disclaimer to the subject matter contained therein.

Claim 2 has been cancelled without prejudice to the subject matter contained therein.

Claims 1, 16, 18 and 19 are amended for "clarification purposes" and no new matter is added or issues raised.

As a preliminary matter, the Examiner objected to the Abstract as not in compliance with proper US practice. A new Abstract of the disclosure is being provided herein.

Further, while an informality has been indicated in the Figure 1, applicants respectfully request that this objection be held in abeyance until such time as allowable subject matter is indicated.

I. Claim Rejections - 35 U.S.C. §112, second paragraph

Claims 1, 3-5 and 16-19 stand rejected under 35 U.S.C. § 112, second paragraph, as allegedly indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regards as the invention.

In this rejection, the Examiner argues that structural interconnection between the process, interface, network scheduler, internal memory and memory manager as recited

in Claim 1 is not clear. Applicants have amended Claim 1 (and similarly, amended Claims 16, 18 and 19 in like manner) to precisely set forth in further clear and definite terms the features/elements of the invention that includes sufficient structure.

Independent device Claim 1, as amended herein, now recites the following clear and definite interrelation of parts:

1. (Currently Amended) A data packet processing device for processing data packets received from a network, comprising:

a processor device for processing data packets;

a memory manager device for initially receiving packets from said network and preloading received data packets to an internal memory coupled therewith, said internal memory for storing packets to be processed by said processor;

an external memory for storing further packets to be processed by said processor;

an interface between said memory manager and said external memory operable for transmitting data packets to and from said external memory;

said memory manager in communication with a scheduler for assigning priority information to each data packet initially received from said network to be pre-loaded to said internal memory which determines an order of the data packets to be processed to each received data packet, and storing links to the data packets in a pointer memory for processing by said processor device in said priority order,

wherein packets with a highest priority that is to be processed and a data

packet that is to be processed next are pre-loaded in said internal memory and data packets with lower priorities are transferred for storage from said internal memory device to said external memory via said interface; and

said memory manager receiving priority information from said scheduler and coupled to the external memory and the internal memory operable to transfer the data packet having the highest priority stored in the external memory to the internal memory to be processed by said processor as one of the next;

wherein the memory manger is operable to transfer a data packet between the internal memory and the external memory via said interface.[Emphasis Added]

Respectfully, no new matter is being entered as full support is clearly found at Figs. 1, 2a and in the specification pages at page 8, line 27 to page 11, line 12 in support thereof..

Applicants note that the underlined portions of the amendment provided herein, recite clear and definite interrelations of parts and, more definitely portray the data-packet flow within the data packet processing device of the invention.

Particularly, the claims are amended to avoid the Examiner's rejection that the flow path of data packets between the recited components is not clear. While the Examiner asserted that it is not clear:

A) Into which memory the data packets just arrived from the network are stored. Applicants in response submit that memory controller element 5 is connected to the processor local bus 4 to receive the data packets from the network 3 and to intermediately

store the received data packet in an internal memory 6 or in an external memory 7. See page 8, line 31 to page 9, line 3 of the description.

B) From which memory the memory controller retrieves the data packets and provides them to the scheduler for priority assignment. Applicants in response submit that each of the received packets is examined upon receipt by scheduler 8 and a priority information is assigned to each of the received data packets. The priority information determines whether a data packet has a high or low priority. See page 9, lines 18-21.

C) Into which memory the data packets are stored after being prioritized by the scheduler. Applicants in response submit that to speed up the data excess by the processor 2, the respective data packet which is actually processed and preferably the data packet which is to be processed next are stored in the internal memory 6. The decision which data packet should be loaded into the internal memory 6, is made by the memory manager 5 according to the information in the pointer memory of the scheduler 8. The processing order determined by the priority information given by the scheduler 8 is provided to the memory manager 5 which then controls the preloading of the respective data packets with the highest priority into the internal memory 6. See page 11, line 22 to page 11, line 1. Also see page 11, lines 3 -12.

D) From which memory the prioritized data packets are retrieved and provided to the processor for processing in according to priority. Applicants in response submit that to speed up the data excess by the processor 2 the respective data packet,

which is actually processed and preferably the data packet which is to be processed next should be stored in the internal memory 6. See page 10, lines 22 – 25.

The claims are amended to avoid the Examiner's rejection that the flow path of data packets between the recited components is not clear.

In view of the above, the Examiner is requested to withdraw the rejection of Claims 1, 3-5 and 16-19 under 35 U.S.C. § 112, second paragraph.

II. Claim Rejections - 35 U.S.C. §103

Claims 1, 3-5 and 16-19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Boyle (USP 5,963,975) in view of Richter (USP 5,623,490).

Applicants respectfully disagree.

While Boyle appears to show a generic Distributed Shared memory system having processors and associated cache element and a shared "main" memory, it does not teach nor suggest use of a scheduler device for assigning priority information. The Examiner applies Richter as providing this teaching. Applicants respectfully disagree.

In applicant's invention, a data packet processor includes memory manager and a scheduler that assigns priority information to each received data packet. The priority information determines an order of the data packets to be processed. The processor also includes an external memory, an internal memory and a memory manager. The memory manager transfers one or more packets with high priority and which are stored in an internal memory of the device to the processor for processing. Further packets having lower priorities are stored in an external memory from said internal memory via an

interface. Thus, in applicant's invention, data packets having the highest priority of all received data packets are transferred to the internal memory by the memory manager to be processed as one of the next.

It is the case that the memory manager also transfers packets from the internal memory back to the external memory (Step S6, Fig. 2a of applicants specification) and also receives higher priority packets from the external memory for storage in the internal memory for processing by the processor device. Particularly, the memory manager receives priority information from said scheduler and coupled to the external memory and the internal memory operable to transfer the data packet having the highest priority stored in the external memory to the internal memory to be processed by said processor as one of the next. (See page 10, lines 12-14 and page 11, lines 3-12 of applicants originally filed specification).

In Richter, referring to Figs. 7A and 7B, and to col. 7 lines 31-52, blocks 708-712 generate packets with priority. Block 714 arranges the packets according to their priority and places the packets in the write WriteQueue 716 in their order of priority. From 716 the packets are sent to either read queue 722 or 724, depending on the identity of the caller. Assuming that the caller is CALLER 2, the packets in read queue 722, which is a buffer memory for storing packets, are forwarded to control means 726, which selects and processes the packets according to their priority. From the above it is clear that Richter neither discloses nor suggests the structure now positively recited in claim 1, that being, in combination, the structure of an external memory, an internal memory, and a memory manager coupled to both the external memory and the internal memory where it

is the memory manager which transfers those packets which are to be processed next from the external memory to the internal memory, and where the memory manager is operable to transfer a data packet from the internal memory back to the external memory.

Claim 1 now recites, in combination, the structure of,

"A data packet processing device for processing data packets received from a network, including ...

a memory manager device for initially receiving packets from said network and preloading received data packets to an internal memory coupled therewith, said internal memory for storing packets to be processed by said processor;

an external memory for storing further packets to be processed by said processor;

an interface between said memory manager and said external memory operable for transmitting data packets to and from said external memory;

said memory manager in communication with a scheduler for assigning priority information to each data packet initially received from said network to be pre-loaded to said internal memory which determines an order of the data packets to be processed to each received data packet, and storing links to the data packets in a pointer memory for processing by said processor device in said priority order,

wherein packets with a highest priority that is to be processed and a data packet that is to be processed next are pre-loaded in said internal memory and data packets with lower priorities are transferred for storage in said external memory from

said internal memory via said interface; and

said memory manager receiving priority information from said scheduler and being coupled to the external memory and the internal memory is operable for transferring the data packet having the highest priority stored in the external memory to the internal memory to be processed by said processor as one of the next;

wherein the memory manger is operable to transfer a data packet between the internal memory and the external memory via said interface. (underscoring added for emphases).

Nowhere does Richter disclose or even suggest the structure that is now positively recited in claim 1, that of a memory manager coupled to both the external and internal memories and operatively transfers only packets with high priority which are to be processed as one of the next from the external memory to the internal memory, and where the memory manager is operable to transfer a data packet from the internal memory to the external memory, as well. For the reasons noted, it is our understanding that claim 1 clearly avoids the combination of Boyle and Richter and is in condition for allowance.

That is, the transfer of data packet content from an internal memory device to the external memory device based upon a priority determination of that packet is not taught nor described in the prior art. That is, Boyle actually teaches away as it is counterintuitive to transfer data packets from a fast "internal" memory (cache) to a slower external memory (e.g. shared memory) processing in the Boyle system.

Claims 3, 4 and 5 depend from claim 1 and, therefore, are also considered to

be in condition for allowance.

Similar amendments have been made to Claims 16, 18 and 19.

Amended claim 16 now recites,

"A method for processing data packets, said method comprising...

receiving, at a data packet processing device, the data packets from a network;

storing, under control of a memory manager device, the received data packets in an internal memory of said data packet processing device;

determining, by a scheduler associated with said memory manager device, a priority of the received data packets and assigning priority information to each of the data packets wherein packets with a highest priority that is to be processed and a data packet that is to be processed next are pre-loaded in said internal memory and data packets with lower priorities are transferred from said internal memory for storage to a memory device external to said data processing device via an interface; and,

storing a pointer link to the data packet in a pointer memory to facilitate processing in the data packet's assigned priority order, and,

receiving, at said memory manager, priority information from said scheduler, said memory manager device coupled to the external memory and the internal memory operable for transferring the data packet having the highest priority stored in the external memory to the internal memory to be processed by said processor as one of the next. (underscoring added for emphases).

Clearly, Richter neither discloses nor suggests transferring a packet having the high priority from the external memory to the internal memory for storage and

processing, in combination with, transferring a packet having a low priority from the internal memory to the external memory which is counterintuitive to cache-based memory data processing systems for reasons mentioned herein above. For this reason it is understood that claim 16 is in condition for allowance. Claim 17 depends from claim 16 and is also in condition for allowance.

For the reason noted above for claim 16, independent claims 18 and 19 are also considered to be in condition for allowance as they have been similarly amended.

CONCLUSION

In view of the above, each of the presently pending claims in this application is believed to be in condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

The Examiner is respectfully requested to contact the undersigned at the telephone number indicated below if the Examiner believes any issue can be resolved through either a Supplemental response or an Examiner's Amendment.

Respectfully submitted,

Steven Fischman
Registration No. 34,594

SCULLY, SCOTT, MURPHY & PRESSER, P.C.
400 Garden City Plaza, Suite 300
Garden City, New York 11530
(516) 742-4343
SF/EW:gc